Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	55604	memory and plurality with blocks	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 10:41
S2	553	S1 and reference adj cell	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 10:41
S3	278	S2 and reference near3 circuits	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 10:42
S4	54	S3 and plurality near sense	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 10:44
S5	213375	nonvolatile or non-volatile or non adj volatile	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 10:44
S6	43	S4 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 11:06
S7	0	S6 and reference adj load	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/26 11:06

transistor 103a of the selection circuit; and a comparator circuit 105 for comparing a voltage output from the reading memory cell 101b and a voltage output from the reference cell 103b.

Summary of Invention Paragraph - BSTX (15):
[0014] In order to perform a reading operation from the reading memory cell 101b, the sense amplifier circuit 100 shown in FIG. 10 can include a charging circuit 106 for providing the drain electrode of the reading memory cell 101b with a bias voltage of the memory cell reading condition, and can also include a charging circuit 107 for providing the drain electrode of the reference cell 103b with a bias voltage of the memory cell reading condition.

Summary of Invention Paragraph - BSTX (17):
[0016] As shown in FIG. 10, a gate voltage to be applied for performing the reading operation (hereinafter, referred to as a "reading gate voltage") is applied to the control gate electrode of the reading memory cell 101b selected by the selection transistor 101a. Simultaneously, a drain voltage to be applied for performing the reading operation (hereinafter, referred to as a "reading drain voltage") is applied to the drain electrode of the selected reading memory cell 101b through the selection transistor 101a by the charging circuit 106, transistor load 102a (FIG. 11) and the resistance load 102b (FIG. 12).

Summary of Invention Paragraph - BSTX (18):
[0017] The charging circuits 106 and 107 operates until the drain electrode of the memory cell 101b and the drain electrode of the reference cell 103b obtain the drain voltage of the memory cell reading condition. After the drain voltage is reached, the charging circuits 106 and 107 stop operating. A source electrode of the selected reading memory cell 101b is grounded through a transistor or the like, and thus a current flows between the drain electrode and the source electrode of the selected reading memory cell 101b (hereinafter, this current will be referred to as a "reading current").

Summary of Invention Paragraph - BSTX (20):
[0019] Substantially the same operation is performed for the reference cell 103b. As a result, a reference current flows between the drain electrode and the source electrode of the reference cell 103b. The reference current is converted into a voltage by the load of the current detection circuit 104, and the voltage is input to the other input end of the comparator circuit 105 (hereinafter, the voltage obtained from the reference current will be referred to as a "reference voltage").

Summary of Invention Paragraph - BSTX (21):
[0020] The reading current of a selected reading memory cell 101b containing electrons in the floating gate electrode, i.e., the program cell, is smaller than the reference current. The reading current is converted into a voltage by

US 20020122336A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2002/0122336 A1

Morikawa (43) Pub. Date: Sep. 5, 2002

(54) REFERENCE VOLTAGE GENERATION THE CIRCUIT FOR SEMICONDUCTOR MEMORY DEVICE, MEMORY READING CIRCUIT INCLUDING SAME, AND ELECTRONIC INFORMATION DEVICE INCLUDING THE SAME

(76) Inventor: Yoshinao Morikawa, Ikoma-shi (JP)

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(21) Appl. No.: 10/077,471

(22) Filed: Feb. 28, 2002

(30) Foreign Application Priority Data

Mar. 1, 2001 (JP) 2001-057499

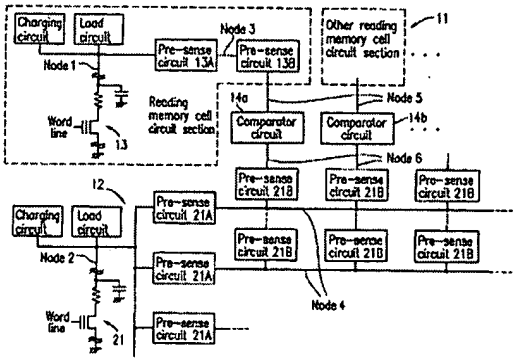
Publication Classification

(51) Int. Cl.[7] G11C 5/00

(52) U.S. Cl. 365/189.09

(57) ABSTRACT

A reference voltage generation circuit includes at least one reference cell having a source electrode and a drain electrode; a plurality of first sense circuits connected to the reference cell and including an N-channel transistor, a P-channel transistor, a plurality of input ends and a plurality of output ends; and a plurality of second sense circuits each for receiving an output from a corresponding one of the plurality of first sense circuits, the plurality of second sense circuits each having a load circuit, an N-channel transistor, a plurality of input ends and a plurality of output ends.



DOCUMENT-IDENTIFIER: US 20040047207 A1

TITLE: Reading circuit, reference circuit and semiconductor memory device

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Abstract Paragraph - ABTX (1):
A reading circuit, for reading data from one memory cell of a plurality of memory cells, includes a plurality of division sensing circuits each connected to the one memory cell via a sensing line corresponding thereto among a plurality of sensing lines; and a current-voltage conversion circuit for converting a current flowing through each sensing line into a sensing voltage representing a potential of the corresponding sensing line. Each division sensing circuit includes a current load circuit for supplying a current to the one memory cell via a corresponding sensing line, and a sense amplifier for sensing a potential difference between the corresponding sensing line and a corresponding reference line of a plurality of reference lines. The current load circuit included in at least one division sensing circuit has a current supply capability different from that of the current load circuit included in another division sensing circuits.

Title - TTL (1):
Reading circuit, reference circuit and semiconductor memory device

Summary of Invention Paragraph - BSTX (3):
[0002] The present invention relates to a reading circuit, a reference circuit and a semiconductor memory device including such a reading circuit and such a reference circuit.

Summary of Invention Paragraph - BSTX (5):
[0004] In general, a reading circuit for reading data from a memory cell array including a plurality of memory cells supplies an electric current to a memory cell having data stored therein, and compares the current (cell current) flowing through the memory cell with a reference current so as to determine whether the level of the cell current is higher or lower than the level of the reference current. Thus, the data written in the memory cell is read. Such a system of reading data is referred to as a "current sensing system".

Summary of Invention Paragraph - BSTX (6):
[0005] For example, data is read from so-called two-level memory cells which can store 1-bit data in one memory cell as described below with reference to FIG. 9B. A first state in which the level of the cell current is higher than that of the reference current (corresponding to data "1"), and a second state in which the level of the cell current is lower than that of the reference

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(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2004/0047207 A1

Mori et al. (43) Pub. Date: Mar. 11, 2004

(54) READING CIRCUIT, REFERENCE CIRCUIT, AND SEMICONDUCTOR MEMORY DEVICE

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(21) Appl. No.: 10/630,566

(22) Filed: Jul. 29, 2003

(30) Foreign Application Priority Data

Jul. 30, 2002 (JP) 2002-221311

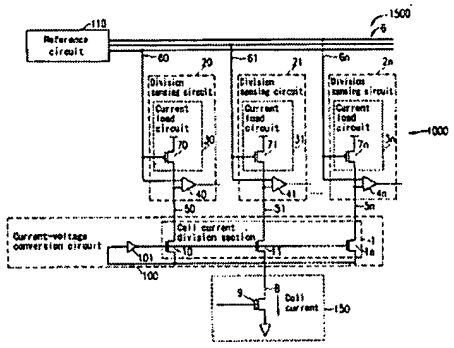
Publication Classification

(51) Int. Cl.[7] G11C 7/00

(52) U.S. Cl. 345/200

(57) ABSTRACT

A reading circuit, for reading data from one memory cell of a plurality of memory cells, includes a plurality of division sensing circuits each connected to the one memory cell via a sensing line corresponding thereto among a plurality of sensing lines; and a current-voltage conversion circuit for converting a current flowing through each sensing line into a sensing voltage representing a potential of the corresponding sensing line. Each division sensing circuit includes a current load circuit for supplying a current to the one memory cell via a corresponding sensing line, and a sense amplifier for sensing a potential difference between the corresponding sensing line and a corresponding reference line of a plurality of reference lines. The current load circuit included in at least one division sensing circuit has a current supply capability different from that of the current load circuit included in another division sensing circuits.



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US-PAT-NO: 6504778

DOCUMENT-IDENTIFIER: US 65047

TITLE: Semiconductor memo

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Find what: reference cell

Area: All / Sel/Cur — Direction: Up / Down — Match word: Whole / Left / Part / Right — Look in: Grid / Documents

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Abstract Text - ABTX (1):

There is provided a semiconductor memory device in which the trouble in reading data due to an overshoot of a data signal can be avoided even when a reference signal for giving a reference for the determination a logical value of the data signal from a memory cell is constantly generated. This semiconductor memory device is constructed such that data is read by comparing a data signal from a memory cell with a reference signal from a reference cell in a differential-type sense amplifier. The semiconductor memory device comprises a feedback circuit for limiting a relative change between the reference signal and the data signal received by the differential-type sense amplifier. This feedback circuit momentarily feeds an output of the differential-type sense amplifier back to its input node, when data stored in the memory cell is read out, to thereby momentarily render the data signal and the reference signal equal to each other.

TITLE - TI (1):

Semiconductor memory device

Brief Summary Text - BSTX (3):

This invention relates generally to semiconductor memory devices such as a flash memory, an EPROM (Erasable and Programmable Read Only Memory) and a ROM (Read Only Memory), and more particularly to a semiconductor memory device of such type that data is read by comparing a data signal from a memory cell with a reference signal/reference voltage from a reference cell.

Brief Summary Text - BSTX (6):

In general, a semiconductor memory device such as a flash memory is constructed so that multi-bit (eight-bit, for example) can be inputted and outputted. A principal structure of a read system in a semiconductor memory device of such type is shown in FIG. 8. As shown in FIG. 8, a memory cell array 1100, comprising non-volatile memory cells (not shown) arranged in a matrix, is divided into blocks 1100-1 to 1100-8 in correspondence with data bits D0 to D7 of external data D, respectively.

Brief Summary Text - BSTX (7):

A plurality of word lines WL are arranged to extend in the row direction of the memory cell array 100 so as to pass through the blocks 1100-1 to 1100-8

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(12) United States Patent
Uekubo

(10) Patent No.: US 6,504,778 B1
(45) Date of Patent: Jan. 7, 2003

(54) SEMICONDUCTOR MEMORY DEVICE

(75) Inventor: Masaki Uekubo, Tokyo (JP)

(73) Assignee: NEC Corporation, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/686,676

(22) Filed: Oct. 11, 2000

(30) Foreign Application Priority Data

Oct. 13, 1999 (JP) 11-291663

(51) Int. Cl.[7] G11C 7/02; G11C 16/06

(52) U.S. Cl. 365/207; 365/210; 365/185.2; 365/185.21

(58) Field of Search 365/185.11, 185.2, 365/185.21, 205, 207, 208, 210; 375/257

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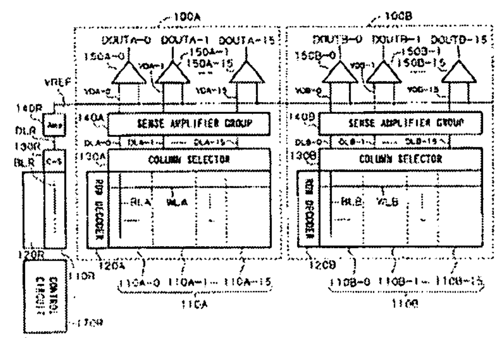
Primary Examiner—Trong Phan

(57) ABSTRACT

There is provided a semiconductor memory device in which the trouble in reading data due to an overshoot of a data signal can be avoided even when a reference signal for giving a reference for the determination a logical value of the data signal from a memory cell is constantly generated. This semiconductor memory device is constructed such that data is read by comparing a data signal from a memory cell with a reference signal from a reference cell in a differential-type sense amplifier. The semiconductor memory device comprises a feedback circuit for limiting a relative change between the reference signal and the data signal received by the differential-type sense amplifier. This feedback circuit momentarily feeds an output of the differential-type sense amplifier back to its input node, when data stored in the memory cell is read out, to thereby momentarily render the data signal and the reference signal equal to each other.

22 Claims, 10 Drawing Sheets



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US-PAT-NO: 5982662

DOCUMENT-IDENTIFIER: US 59826

TITLE: Semiconductor memo
characteristics for data h

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Find what: reference cell

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Abstract Text - ABTX (1):
A semiconductor memory device is described that has an improved read characteristics. The semiconductor memory device includes a plurality of memory cells, a reference cell, a comparator located between the memory cells and the reference cell, and a discriminator coupled to the comparator. The comparator compares the actual signal equivalent to a value of a current flowing in each of the memory cells and reference signals equivalent to a value of a current flowing in the reference cell with each other to output a comparison result signal in each of data reading operation modes. The discriminator discriminates a value of data stored in each of the memory cells based on the comparison result signal. The discriminator includes a circuit shared for discrimination of a data value in each of the data reading operation modes.

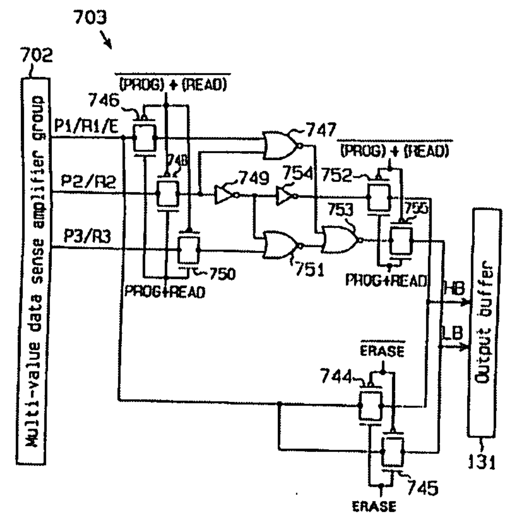
TITLE - TI (1):
Semiconductor memory device with improved read characteristics for data having multi values

Brief Summary Text - BSTX (3):
The present invention relates generally to a semiconductor memory device. More particularly, this invention relates to a flash EEPROM (Electrical Erasable and Programmable Read Only Memory) with improved read characteristics for data having multi values.

Brief Summary Text - BSTX (5):
Considerable attention has recently been given to non-volatile semiconductor memories, such as a ferro-electric memory, EPROM (Erasable and Programmable Read Only Memory) and EEPROM (Electrically Erasable and Programmable Read Only Memory). To store data, an EPROM and EEPROM use a floating gate for storing charges and a control gate for detecting a change in threshold voltage according to the presence or absence of charges in the floating gate. EEPROMs include a flash EEPROM which can perform data erasure for the entire memory chip or partial data erasure for each of a plurality of blocks in the memory cell array. There are two general types of memory cells in a flash EEPROM: a split gate type and a stacked gate type.

U.S. Patent Nov. 9, 1999 Sheet 21 of 23 5,982,662

Fig.21



having I-V circuit